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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,815	07/21/2003	Marco Troost	P2001,0034	5766

24131 7590 10/28/2005

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,815	TROOST, MARCO	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 5-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiga (5,416,660) in view of Chrysostomides et al. (5,646,434) and Takamoto et al. (5,079,612).

Shiga teach in figure 2a and related text a semiconductor component comprising: a semiconductor chip 7 including an electronic circuit configured therein, said electronic circuit having a terminal for a signal to be processed, said electronic circuit having a stage connected to said terminal for the signal, said electronic circuit having a terminal for obtaining a supply potential 6, said terminal for obtaining the supply potential being connected to said stage, said stage selected from a group consisting of an input stage and an output stage;

a first conductor track running outside said semiconductor chip, said first conductor track being connected to said terminal for the signal;

a second conductor track running outside said semiconductor chip, said second conductor track being connected to said terminal for obtaining the supply potential;

a further conductor track 6 running outside said semiconductor chip, said further conductor track being connected to said second conductor track;

an ESD protection element 2 for carrying an electrostatic discharge away from said terminal for the signal and to the supply potential, said ESD protection element for carrying the electrostatic discharge disposed outside of said semiconductor chip; and

said ESD protection element for carrying the electrostatic discharge connected (at least electrically connected) outside of said semiconductor chip to said further conductor track (power supply) and to said first conductor track.

Shiga does not teach a stage selected from a group consisting of an input stage and an output stage, and a further conductor track surrounds said semiconductor chip.

Chrysostomides et al. teach in figures 1 and 5 and related text a stage selected from a group consisting of an input stage and an output stage, and a further conductor track 23 surrounds said semiconductor chip, wherein bonding wires 9 and 6 of first conductor track and second conductor track cross said further conductor track, thus defining a crossing location wherein said ESD protection element being disposed close to said crossing location.

Takamoto et al. teach in figure 1 and related text a further conductor track 21, 22 surrounds a semiconductor chip, wherein bonding wires of first conductor track and second conductor track cross said further conductor track, thus defining a crossing location wherein said ESD protection element being disposed close to said crossing location.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a stage selected from a group consisting of an input stage and an output stage and a further conductor track surrounds Shiga's semiconductor chip, in order to use the device in an application which requires an ESD protection to an input and an output stage of the chip, and in order to improve the noise characteristics of the device and to simplify the external connections to the device by providing a further conductor track surrounding the semiconductor chip, respectively.
Regarding the claimed limitations of a further conductor track crossing said first conductor track, thus defining a crossing location and said further conductor track crossing said second conductor track, wherein said ESD protection element being disposed close to said crossing location, these features are inherent in prior art's device because since the further conductor track surrounds the semiconductor chip, it must cross said first conductor track, thus defining a crossing location and it must cross said second conductor track. The ESD protection element is inherently disposed close to said crossing location.

Regarding claim 2, Shiga teaches in figure 2a and related text a package surrounding said semiconductor body and said further conductor track; said package partially surrounding said first conductor track such that a portion of said first conductor track facing toward said semiconductor chip runs inside said package and a portion of said first conductor track facing away from said semiconductor chip runs outside said package; and

said package partially surrounding said second conductor track such that a portion of said second conductor track facing toward said semiconductor chip runs inside said package and a portion of said second conductor track facing away from said semiconductor chip runs outside said package.

Regarding claim 3, Shiga teaches in figure 2a and related text said ESD protection element is a diode; said diode has an anode connected to said further conductor track; and said diode has a cathode connected to said first conductor track.

Regarding claim 5, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an insulation material configured where said further conductor track crosses said first conductor track in Shiga's device, in order to avoid short circuit the device.

Regarding claim 6, Chrysostomides et al. teach in figure 5 a third conductor track Vcc2; a terminal for a signal and assigned to said third conductor track; and a further element 13, 15 for carrying an electrostatic discharge; said further conductor track running in a main direction and having a conductor track portion branching away from said main direction; said third conductor track crossing said further conductor track near said conductor track portion of said further conductor track (via wiring 8); and said conductor track portion of said further conductor track is connected to said further element for carrying the electrostatic discharge.

Regarding claims 7-8, Chrysostomides et al. teach in figure 5 a bonding wire connecting said first conductor track to said terminal for the signal; and a bonding wire connecting said second conductor track to said terminal for obtaining the supply potential, wherein said terminal for the signal and said terminal for obtaining the supply potential are metallized areas configured in said semiconductor body.

Regarding claim 9, Chrysostomides et al. teach in figure 5 an input stage has at least one transistor with a gate connected to said terminal for the signal; said transistor has a drain terminal and a source terminal; said drain terminal or said source terminal of said transistor connected to said terminal for the supply potential.

Regarding claim 10, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an inverter as the input stage in Shiga's device in order to use the device in an application which requires an inverter.

Regarding claim 11, Shiga teaches in figure 2a and related text claim 1 a package wall disposed outside said semiconductor chip and including said first conductor track, said first conductor track having a contact area connected to a terminal of said electrostatic discharge protection element. Shiga does not teach a package wall comprising a lead frame. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a lead frame in Shiga's device in order to use simplify the processing steps of making the device by using conventional packaging material.

Regarding claim 12, Shiga teaches in figure 2a and related text said first conductor track is connected to said terminal for the signal through a bonding wire.

Response to Arguments

Applicant argues that Chrysostomides et al. and Takamoto et al. do not teach a further conductor track running outside said semiconductor chip, because Chrysostomides et al. and Takamoto et al. teach a further conductor track running inside said semiconductor chip. Applicant further argues that it is unclear what is meant by the examiner's comment that "the broad recitation of the claim does not exclude the further conductor track 23 from being an integrated conductor track and running within an integrated circuit".

Claim 1 recites a further conductor track running inside said semiconductor chip. Chrysostomides et al. and Takamoto et al. teach a further conductor track running surrounding a semiconductor chip. Although it is possible that prior art indicate that other parts of the integrated circuit are located outside the further conductor track, this does not prevent the further conductor track 23 from surrounding the semiconductor chip and thus from running outside said semiconductor chip. Again, "the broad recitation of the claim does not exclude the further conductor track 23 from being an integrated conductor track and running within an integrated circuit". That is, applicant does not claim that other parts of the integrated circuit can not be located outside the further conductor track. A recitation such as "a further conductor track running outside

the entire components/circuits/stages of said semiconductor chip", would overcome the rejection as recited in this office action.

Applicant argues that Chrysostomides et al. cannot be used to argue obviousness of the crossing location of claim 1 of the instant application, because the crossing location of the invention of the instant application is defined between the further conductor track and the first conductor track which is a conductor track for a signal (rather than for a supply potential for which bonding wires 6, 9 of Chrysoatomides et al. are intended).

Chrysostomides et al. is not used to argue obviousness of the crossing location of claim 1 of the instant application. Chrysostomides et al. is cited to teach an artisan the obviousness of a further conductor track surrounding a semiconductor chip and having crossing locations with external wires. Shiga teaches a first conductor track which is a conductor track for a signal.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
10/26/05

ORI NADAV
PRIMARY EXAMINER
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